AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): ~~Method~~A method, for storing register properties of ~~a~~an hardware device ~~(ASIC1, ASIC2, ASIC3, ASIC4)~~ having heterogeneous memory in a datastructure, said hardware device ~~(ASIC1, ASIC2, ASIC3, ASIC4)~~ being built according to a structure of modules and dependent sub-modules, wherein said register properties correspond to register properties of said modules and said sub-modules, ~~characterised in that~~ wherein said method comprises: ~~the step of~~

storing said register properties in a data-structure according to said structure of said hardware device, ~~(ASIC1, ASIC2, ASIC3, ASIC4)~~ said register properties being arranged in an array for each module or dependent sub-module.

2. (currently amended): ~~Data~~ A data structure ~~for holding~~ comprising register properties of an hardware device having heterogeneous memory ~~(ASIC1, ASIC2, ASIC3, ASIC4)~~, said hardware device ~~(ASIC1, ASIC2, ASIC3, ASIC4)~~ being built according to a structure of modules and dependent sub-modules, wherein said register properties correspond to register properties of said modules and said sub-modules, ~~characterised in that~~ wherein said data-structure is adapted to hold said register properties in a structure according to said structure of said hardware device, and ~~(ASIC1, ASIC2, ASIC3, ASIC4)~~ wherein said register properties are arranged in an array for each module or dependent sub-module.

3. (original): Data-structure according to claim 2, characterised in that said array corresponding to a module of said hardware device comprises a number of repetitions indicator, adapted to indicate the number of reoccurrences of a submodule of said module.

4. (previously presented): Data-structure according to claim 2, characterised in that said device properties in each said array includes either one of an initial value of a register, the read-write bits, unstable read-write bits or read-reset bits.

5. (previously presented): Data structure according to claim 2, characterised in that said data-structure is held by a storage device.

6. (previously presented): Data structure according to claim 2 for use in access test executed by a generic test device.

7. (original): Data structure according to claim 6, characterised in that said access tests of said ASIC include either one of Read/Write of multiple patterns to two registers, data-bus test, address-bus test, device reset test or test initial values of all registers.